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Respectfully submitted,

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Version With Markings To Show Changes Made

IN THE SPECIFICATION:

The paragraph heading has been inserted on page 1 of the English translation of the subject application, before line 5, as follows:

Technical Field

The paragraph heading has been inserted on page 1 of the English translation of the subject application, before line 9, as follows:

Related Art

The paragraph heading has been inserted on page 5 of the English translation of the subject application, before line 5, as follows:

Summary of the Invention

The paragraph heading has been inserted on page 8 of the English translation of the subject application, before line 25, as follows:

Detailed Description of the Invention

IN THE CLAIMS:

The paragraph heading "Patent Claims" has been deleted and the paragraph heading has been inserted in place thereof on page 16 of the English translation of the subject application, as follows:

CLAIMS

The paragraph heading has been inserted on page 16 of the English translation of the subject application, before claim 3, as follows:

What is claimed is:

1. (Amended) A high speed processor having:

a data processing unit [(13)] for processing data;

a data memory [(20)] which is connected to the data processing unit via a data bus [(10)] and can be addressed by the data processing unit [(13)] via a data memory address bus [(18)];

at least one input interface buffer [(9)] which is connected to the data bus [(10)] and has the purpose of buffering input data;

at least one output interface buffer [(26)] which is connected to the data bus [(10)] and has the purpose of buffering output data;

the input interface buffer [(9)] and the output interface buffer [(26)] being directly addressable by the data processing unit [(13)] via an interface address bus [(24)].

2. (Amended) The high speed processor as claimed in claim 1, wherein the data memory [(20)] contains at least one RAM memory [(19)].

3. (Amended) The high speed process as claimed in claim 1 [or 2], wherein the data processing unit [(13)] is connected to the ROM memory [(15)] which stores program data.

4. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the data processing unit [(13)] is an RISC data processing unit.

5. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the data processing unit [(13)] contains a plurality of addressable internal registers.

6. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the data processing unit [(13)] can carry out a plurality of data transfer processor commands in order to directly exchange data between the data memory [(20)], the registers [(14)] and the interface buffers [(9, 26)].

7. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein when a first data transfer processor command is carried out by the data processing unit [(13)], the input data buffered in the input interface buffer [(9)] is transmitted directly into an internal register [(14)] for data processing.

8. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein when a second data transfer processor command is carried out by the data processing unit [(13)], the input data buffered in the input interface buffer is transmitted directly into an output interface buffer [(26)] for the outputting of data.

9. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein when a third data transfer processor command is carried out by the data processing unit [(13)], the data buffered in an internal register [(14)] of the data processing unit [(13)] is transmitted directly into the output interface buffer [(26)] for the outputting of data.

10. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein when a fourth data transfer processor command is carried out, the input data buffered in an input interface buffer [(9)] is transmitted directly into the data memory [(20)] for storage.

11. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein when a fifth data transfer processor command is carried out by the data processing unit [(13)], the data stored in the data memory [(20)] is transmitted directly into the output interface buffer [(26)] for the outputting of data.

12. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the input interface buffer [(9)] is connected to an analog/digital converter [(5)].

13. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the output interface buffer [(26)] is connected to a D/A converter [(32)].

14. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the input interface buffer [(9)] and the output interface buffer [(26)] are connected to the data processing unit [(13)] via a control signal bus.

15. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the input interface buffer [(9)] is an xDSL interface buffer for buffering xDSL data.

16. (Amended) The high speed processor as claimed in claim 15, wherein the xDSL input interface buffer [(9)] has a data frame detecting device for detecting a data frame synchronization data pattern.

19. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the output interface buffer [(26)] is a PCM interface buffer for buffering PCM data.

20. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein each internal register [(14)] has a plurality of memory locations for different data words.

21. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein each processor task executed by the data processing unit [(13)] is assigned a separate internal register.

22. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein peripherals can be connected to the interface buffers [(9, 26)].

23. (Amended) The high speed processor as claimed in [one of the preceding claims] claim 1, wherein the input interface buffer [(9)] and the output interface buffer [(26)] can be configured.